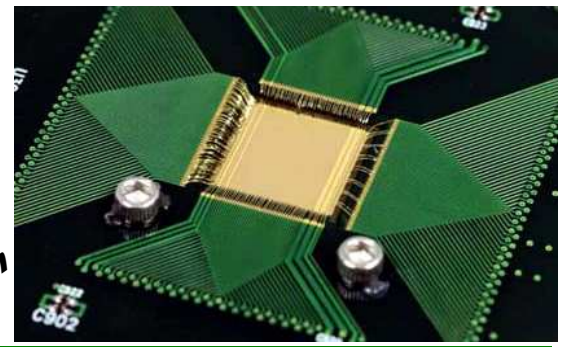


Evolutionary Computation in Network-on-Chip Based Systems



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Paper Submission:
1/11/2008

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16/01/2009

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Description and Motivation:

Network-on-Chip (NoC) is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. It is used as a new approach to designing complex System-on-a-chip (SoCs) design. NoC-based systems can accommodate multiple complex SoC designs. In a NoC-based system, modules such as processor cores, memories and specialized IP blocks exchange data using a on-chip network. An NoC is constructed from multiple point-to-point data links interconnected by switches also called routers, such that messages can be relayed from any source module to any destination module over several links, by making routing decisions at the switches.

VLSI designers of NoC-based systems face several problems, among which we can cite, for instance, planning the architecture that is most suitable to a given application is order to improve performance and mapping the sub-systems that form the application into a multiple nodes of the NoC architecture. Evolutionary computation can be used as a very robust tool to bring some answers to this kind of design problems.

The aim of this special session is to bring together hardware, middleware and application designers that exploit the evolutionary computation principles to provide CAD tools for NoC-based systems. This session will allow researchers to share experiences and identify theoretical and technical issues in this field of expertise. Submitted papers may describe applications, computing models, modeling frameworks, or hardware platforms and architecture.

Submission Guidelines

Manuscript should be prepared according to the standard format of regular paper specified for IEEE CEC 2009. Paper submission is done online through the CEC 2009 submission system (<http://www.cec-2009.org>). Papers submitted to this special session will be peer-reviewed with the same criteria used for other contributed papers. All accepted papers will be published in the conference proceedings.

Post-Conference Publication

Extended version of some selected papers of high-quality will be recommended for publication in: International Journal of Innovative Computing and Applications (<http://www.inderscience.com/ijica>) and International Journal of High Performance Architecture Systems (<http://www.inderscience.com/ijhpsa>).